IN THE CLAIMS

Claim 1 (Currently Amended): A semiconductor integrated circuit, comprising:

a shielded wire line; and

a shielding wire line provided for the shielded wire line, wherein a width of the shielding wire line is greater than ~~and having~~ a width ~~broader than that~~ of the shielded wire line, and each of the shielding wire line and the shielded wire line are positioned within a same layer of the semiconductor integrated circuit.

Claim 2 (Withdrawn): A semiconductor integrated circuit, comprising:

a shielded wire line; and

a plurality of shielding wire lines provided for the shielded wire line on one side of the shielded wire line.

Claim 3 (Withdrawn): A semiconductor integrated circuit, comprising:

a shielded wire line; and

a shielding wire line provided along only a portion of an entire extent of the shielded wire line.

Claim 4 (Withdrawn): The semiconductor integrated circuit as claimed in claim 3, further comprising a driver that transmits a signal to the shielded wire line, wherein the portion of the entire extent of the shielded wire line along which the shielding wire line is provided is a portion on a side of the driver.

Claim 5 (Withdrawn): A method of determining wire lines of a semiconductor

integrated circuit, comprising the steps of:

providing as a library, shielding effects of partial shielding that shields only a portion of an entire extent of a shielded wire line;

determining a length of the shielded wire line;

determining a desired shielding effect; and

determining a length of a shielding wire line by looking up the length of the shielded wire line and the desired shielding effect in the library.

Claim 6 (Withdrawn): The method as claimed in claim 5, wherein the step of providing as a library the shielding effects of partial shielding provides, as the library, information about signal delay time that appears when a portion of the entire extent of the shielded wire line is shielded.